ST. ALOYSIUS COLLEGE(AUTONOMOUS), JABALPUR

Reaccredited 'A+ 'Grade by NAAC(CGPA:3.68/4.00)
College with Potential for Excellence by UGC
DST-FIST Supported & STAR College Scheme by DBT

Faculty of Science

Bachelor of Computer Application

BCA I Semester

Paper-Major

COMPUTER FUNDAMENTAL ORGANIZATION AND ARCHITECTURE

Course Outcomes

CO. No.	Course Outcomes	Cognitive Level
CO 1	Understand the basic structure, operation and characteristics of digital computer.	U
CO 2	Be able to design simple combinational digital circuits based on given parameters.	Apply
CO 3	Understand the working of arithmetic & logic unit.	Apply, Analyze
CO 4	Know about hierarchical memory system including cache memories and virtual memory.	Create, Apply
CO 5	Understand concept and advantages of parallelism, multi-processors and multi-core processors.	Apply

Credit and Marking Scheme

	Credits	Marks		Total Marks
		Internal	External	
Theory	3	40	60	**100**
Practical	1	40	60	**100**
Total	**4**	**200**		

Evaluation Scheme

	Marks	
	Internal	**External**
Theory	3 Internal Exams of 20 Marks (During the Semester) (Best 2 will be taken)	1 External Exams (At the End of Semester)
Practical	3 Internal Exams (During the Semester) (Best 2 will be taken)	1 External Exams (At the End of Semester)

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BCA I Semester **Paper-Major**

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Theory

No. of Lectures (in hours per week): 2 Hrs. per week

Total No. of Lectures: 60 Hrs. **Maximum Marks:** 60

Units	Topics	No. of Lectures
I	Fundamentals of Computer – Definition, Characteristics, Block Diagram of a Computer, Input devices - Output Devices- Keyboard, Scanner, Mouse, light pen, Bar Code Reader, OMR, OCR, MICR, Printers- types of Printer, Monitors, Plotters-types of plotters, Computer Memory- Types of Memory.	15
II	Fundamentals of Digital Electronics: Number System-Binary, Decimal, Octal, Hexa-Decimal, Conversions, Binary Arithmetic-Addition, Subtraction, Multiplication, Division, Underflow, Overflow, Sign Magnitude, Complements-1's and 2's, Fixed-Point Representation, Floating-Point Representation.	15
III	Boolean Algebra, Reducing Boolean Expression, Logic Gates-AND, OR, NOT, Universal Gates-NAND, NOR, Analog and Digital Signals, Clock Waveform Timing, Map Simplification, K-Map- Two, Three and Four variables.	15
IV	Combinational Circuits- Adder, Subtractor, Multiplexer, De-multiplexer, Decoders, Encoders. Binary Codes – Gray Codes, ASCII code, BCD code, EBCDIC, Error Detection Code and Correction Code, Hamming Code.	15
V	Sequential Circuits - Flip - Flops, SR, D, T, JK, Master-Slave, Registers, Shift Registers- SISO, SIPO, PISO, PIPO, Counters, Instruction, Instruction Format, Instruction Codes, Handshaking, DMA Data Transfer, Auxiliary Memory, Cache Memory, Associative Memory, Flynn's classification - Introduction to SISD, SIMD, MISD, MIMD, Parallelism, Multicore processors.	15

Textbook:

- "Computer system Architecture" by M.Morris Mano, Pearson
- "Computer system Architecture and Organization" by Patterson, McGraw Hill
- "computer system Architecture & Organization" Sps Saini, S.K.KAtheria, Published by Katharia and Sons

Suggestive digital platform web links

- https://web.iitd.ac.in/-minati/MTL458.html
- https://www.cse.iitb.ac.in/-mythili/os/https://www.youtube.com/watch?v=aCJ3YgHQ

Suggested Equivalent online courses

- https://nptel.ac.in/courses/106/102/106102132

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List of Practical

PART-1 (Computer Fundamentals)

1. Various parts of a Computer
2. Identify various parts inside the CPU like motherboard, SMPS, Ports, Buses, IC chip, Processor, HDD, RAM.
3. Identify various I/O devices

PART-II (Digital Electronics)

1. To study basic gates (AND, OR, NOT) and verify their truth tables.
2. To study and verify NAND as Universal gate using IC 7400.
3. To realize basic gate AND from Universal gate NAND.
4. To realize basic gate OR from Universal gate NAND.
5. To realize basic gate NOT from Universal gate NAND.
6. To study and verify NOR as Universal gate.
7. To realize basic gate AND from Universal gate NOR.
8. To realize basic gate OR from Universal gate NOR.
9. To realize basic gate NOT from Universal gate NOR.
10. Verification and Interpretation of truth table for XOR gate.
11. To study Half Adder using basic gates and verify its truth table.
12. To study Full Adder using basic gates and verify its truth table.
13. To design and construct RS flip Flop using gates and verifies the truth table.
14. To design and construct JK Flip Flop using gates and verifies the truth table.
15. To verify De-Morgan's First Law Theorem.
16. To verify De-Morgan's Second Law Theorem.